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Technology, Hisar, India (e-mail: arya1sandeep@rediffmailcom) Dr Sujata Pandey is with the Department of Electronics & Communication Engineering, Amity University, Noida, India (e-mail: spandey@amityedu) Addition of two binary numbers is fundamental and most frequently used arithmetic operation in microprocessors,

International journal of computer science & information ...
International journal of computer science & information Technology (IJCSIT) Vol2, No5, October 2010 Sandeep K Arya 1, Sujata Pandey 2 VLSI circuits and system [1], [2] With increase in

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Vipul Bhatnagar faculty profile
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Lowpowerdigitallycontrolledoscillatordesignswithanovel3 ...
JSemicond2012,33(3) ManojKumaret al Table5Phasenoise,RMSvalueofoutputsignalandphasenoisecutofffrequencyresultsforproposedDCOcircuits DCOcircuit Phasenoise@1MHz

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very large-scale integration (VLSI) application The power consumption of the circuit is in range of 4217256uw to 581542uw in 035 um technology with a voltage supply range of 18V to 33V The simulation process has performed by the SPICE and DSCH tool Sandeep K Arya and Sujata pandey…

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High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design," in International Journal of VLSI design & Communication Systems (VLSICS) Vol3, No2, April 2012 [6] Manoj Kumar, Sandeep K Arya and Sujata Pandey, Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate in

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IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 6, Issue 2, Ver In this section as a comparative analysis using 45nm Cadence GPDK technology the conventional level Sujata Pandey, "Level Shifter Design for Low Power Applications", International Journal of

Single bit full adder design using 8 transistors with ...

Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate Manoj Kumar 1, Sandeep K Arya 1 and Sujata Pandey 2 1Department of Electronics & Communication Engineering Guru Jambheshwar University of Science & Technology, Hisar, 125 001, India 2Amity University, Noida, 201303, India Abstract:

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Voltage Controlled Ring Oscillator Design with Novel 3 ...

er consumption in very large scale integration (VLSI) systems includes dynamic, static power and leakage power consumption Dynamic power consumption re-sults from switching of load capacitance between two different voltages and dependent on frequency of opera-tion Static power is contributed by direct path short cir-

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Power Optimization of Communication System Using Clock Gating Technique Kanika Sahni Kiran Rawat Sujata Pandey Ziauddin Ahmad Amity University Noida Uttar Pradesh, India Amity University Noida Uttar Pradesh, India This is the main task for the VLSI engineers and …

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engineering and technology hello_yashpatel@yahoocom Mr Rahulkumar Jha Dept of Electronics Thakur college of engineering and technology rahuljha0609@gmailcom Mrs Sujata Alegavi Dept of Electronics Thakur college of engineering and technology sujatadubal@thakureducationorg Abstract -Livestock Management is a laborious task as the

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2 and Sujata Pandey3 1* power conservation has become major design concern for very large scale integration (VLSI) circuits and system design (Leblebici Kumar et al / International Journal of Engineering, Science and Technology, Vol 2, No 6, 2010, pp 297-304 298

ONE BIT 8T FULL ADDER CIRCUIT USING 3T XOR GATE AND ...

Gate,Manoj Kumar, Sandeep K Arya, and Sujata Pandey [3] NWeste and kEshranghaian 'Principles of CMOS VLSI Design: A system perspective'' Reading MA Addison-wesley 1993 [4] Fayed and M Bayoumi, "A low-power 10-transistor full adder cell for embedded architectures," in Proc IEEE Symp

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Technology and Science (ICCTS 2014) organized by IACSIT held in the Sarawak, Malaysia on 7-8, June, 2014) 22 AKGupta, SGovinda," Design of low voltage rail to rail voltage to frequency converters for portable applications" Proceedings of the National Conference on VLSI, Signal Processing and