Digital Design Final Exam And Answers

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Digital Design Final Exam And

Sample Final Exam Solutions - University of Idaho
COE/EE 243 Digital Logic Session 44; Page 1/5 Spring 2003 COE/EE 243 Sample Final Exam From Fall 98 Solutions Show your work Do NOT use a calculator! 1 (9 pts) Complete the following table of equivalent values

Digital Logic Design Final Examination
The University of Toledo s18fs_dild7fm - 2 EECS:1100 Digital Logic Design Dr Anthony D Johnson Student name _____ Problem 1 12 points Given is a logic (switching) function F 1 in the decimal list sum-of-minterms representation (1-1) Problem statement

Digital Logic Design Final Examination
The University of Toledo s17fs_dild7fm - 2 EECS:1100 Digital Logic Design Dr Anthony D Johnson Student name _____ Problem 1 12 points Given is a logic (switching) function F 1 in the decimal list sum-of-minterms representation (1-1) Problem statement

CSE 260 – Introduction to Digital Logic and Computer ...
CSE 260 – Introduction to Digital Logic and Computer Design Jonathan Turner Final Exam Solution 5/7/2014 - 2 - 2 (10 points) Use the Karnaugh map below to find a minimum sum-of-products expression for Σ m(0,1,3,4,5,8,9,12,14) How many simple gates of each type are needed to implement this

14:332:231 DIGITAL LOGIC DESIGN
DIGITAL LOGIC DESIGN Ivan Marsic, Rutgers University Electrical & Computer Engineering Fall 2013 2o 3f 0 Organizational Matters (1) – Midterm Exam 2 20 % (~Nov 19 or 27) – Final Exam 30 % – Random Quizzes 10 % 3 5o 3f 0 Source: Wikipedia 6o 3f 0 Source: Wikipedia 4 7o 3f 0 Clock Rate Grows Exponentially Year 1 10 100 1,000

Written exam with solutions IE1204-5 Digital Design Friday ...

Written exam with solutions IE1204-5 Digital Design Friday 15/1 2016 1400-1800 General Information at the rest of your exam Part B (Design problems) contains two design problems of a total of 10 points Part B is outcomes on a digital number display The display

ENEL 353 - Digital Circuits Final Examination

ENEL 353 Final Examination - Fall 2008 Page 11 of 12 4 [24 marks total] Design a sequential binary adder Two binary sequences of an arbitrary length, corresponding to the two operands to be added, are applied to the inputs A and B, where the least-signi cant bit (LSB) of each sequence arrives rst

ECE/CS 352 Digital System Fundamentals Final Exam Solution

ECE/CS 352 Final Exam May 12, 2002 9 6 (10 points) One-flip-flop-per-state implementation Below is an ASM chart of a certain controller Implement this ASM chart using one-flipflop-per-state method Using positive edge triggered flip-flops, AND, OR, NOT gates Simplify the design to use as few logic gates as possible Answer: Idle S0 G 0 1

Written exam with solutions for IE1204/5 Digital Design ...

1 Written exam with solutions for IE1204/5 Digital Design Monday 27/10 2014 900-1300 General Information Examiner: Ingo Sander Teacher: Elena Dubrova /William Sandqvist, tel 08-7904487

Final Exams Review - University of Waterloo

Final Exams Review Spring 2011 Should you have any questions on this review, please contact Arash [aTabibiazar@uwaterlooca] ECE124 Digital Circuits and Systems, Final Review, Spring 2011 Should you have any questions on this review, please contact Arash Design a digital circuit that takes two 4 -bit numbers A and B as input and

Solutions

ICS 151 Digital Logic Design, Spring Quarter 2006, Final Page 8 Q2: FSM Design – Moore and Mealy Machines [30 points] We want to design a non-resetting sequence detector using a finite state machine with one input X and one output Y The FSM asserts its output Y when it recognizes the following input bit sequence: "1101"

EE 110 Practice Problems for Final Exam: Solutions

EE 110 Practice Problems for Final Exam: Solutions, Fall 2008 5 NOT AND OR AND OR OR AND AND AND XOR CLK x z J2 +5V K2 Q2 Q2 J1 K1 Q1 Q1 J0 K0 Q0 Q0 2 State Bubble Diagram of Mealy Machine Redraw the state bubble diagram using a Mealy machine design Be sure to label the transitions and bubbles You may name your states whatever you like

Decoders, Encoders, Multiplexers, Demultiplexers ...

EECC341 - Shaaban #6 Final Review Winter 2001 2-20-2002 Encoders • If the a decoder's output code has fewer bits than the input code, the device is usually called an encoder eg 2n-to-n, priority encoders • The simplest encoder is a 2n-to-n binary encoder, where it has only one of 2n inputs = 1 and the output is the n-bit binary number corresponding to the active input

Digital Logic I EE 2720-2 Midterm Examination

Digital Logic I EE 2720-2 Midterm Examination 102 9 November 2011, 14:40–15:30 CST Exam Rules Use only a pencil or pen No calculators of any kind are allowed Texting is out of the question Alias Saila Problem 1 (22 pts) Problem 2 (22 pts) Problem 3 (22 pts) Problem 4 (12 pts) Problem 5 (12 pts) Problem 6 (10 pts) Exam Total (100 pts) Good

EE 110 Practice Problems for Exam 2: Solutions, Fall 2008

EE 110 Practice Problems for Exam 2: Solutions, Fall 2008 3 3 Combinational Logic: Design a circuit that counts the number of 1's present in 3 inputs A, B and C Its output is a two-bit number X1X0, representing that count in binary Assume active-HIGH logic 3(a) Write the truth table for this circuit Solution: A B C X1 X0 0 0 0 0 0 0 0 1

Understanding Logic Design - University of Iowa

Understanding Logic Design Appendix A of your Textbook does not have the needed background information This document supplements it When you write add ADD R0, R1, R2, you imagine something like this: R1 R0 R2 What kind of hardware can ADD two binary integers? We need to learn about GATES and BOOLEAN ALGEBRA that are foundations of logic design

Digital Marketing MKT 382 Course Syllabus

(MKT 460) and Digital Marketing (MKT 372, MKT 382) at McCombs Prior to his graduate work, Professor Bentley worked in Hollywood producing movie trailers and TV commercials for upcoming films He proceeded to earn both his PhD and MBA from Washington University in St Louis and a BA from Principia College

Faculty of Engineering ELECTRICAL AND ELECTRONIC ...

Introduction to Logic Design/ Digital Logic Design I - Final Examination Question 7 (15 points): Use JK flip flops to design a counter with the repeated binary sequence:0,1,2 The circuit is to be designed by treating the unused states as don't care conditions

Introduction to Digital Logic with Laboratory Exercises

require vast amounts of engineering in their design, they all share the ubiquitous bit as their fundamental unit of data In essence it all starts with TRUE and FALSE or 0 and 1 And so the next chapter starts with the simplest of Introduction to Digital Logic with Laboratory Exercises

SYLLABUS 29-Oct-08 7 EEL 4712: DIGITAL DESIGN

Basic digital design and a working knowledge of one high level programming language (such as FORTRAN, BASIC, PASCAL or C) and an acquaintance with assembler language are assumed TEXTBOOK AND SOFTWARE Brown, S D and Vranesic, Z G, "Fundamentals of Digital Logic with VHDL Design with CD-ROM, 2nd Edition", McGraw-Hill, 2005